**Lab 2: Analog to Digital Converter**

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**Bench** 02

**Electronics** II Lab

**EECE.3120 803**

**Date submitte**d 09/20/2022

**Due date** 09/21/2022

1. **SUMMARY**

In this lab we perform series of experiments using an analog to digital converter (ADC) to gain experience in this universal IC and to learn how it interacts with other circuit components.

1. **EQUIPMENT**

**Table 1. Equipment**

|  |  |  |
| --- | --- | --- |
| **Equipment Type** | **Details** | |
| * Oscilloscope | *Make:* | Tektronix |
| *Model:* | MDO3014 |
| *Serial Number:* | CO44915 |
| * Digital Multimeter | *Make:* | Keithley |
| *Model:* | 2110 5½ |
| *Serial Number:* | 8007691 |
| * DC Power Supply | *Make:* | Keithley |
| *Model:* | 2231A-30-3 |
| *Serial Number:* | Unable to acquire |
| * Function Generator | *Make:* | Tektronix |
| *Model:* | AFG1022 |
| *Serial Number:* | 1731386 |
| * Analog Discovery | *Make:* | Digilent |
| *Model:* | Analog Discovery 2 |
| *Serial Number:* | 210231B0DF82 |
| * Handheld Digital Multimeter | *Make:* | Tenma |
| *Model:* | 72-9385 |
| *Serial Number:* | H200487467 |
| * Breadboard * Bench “Shoebox” with connector cables, adapters, clips etc. | N/A | |

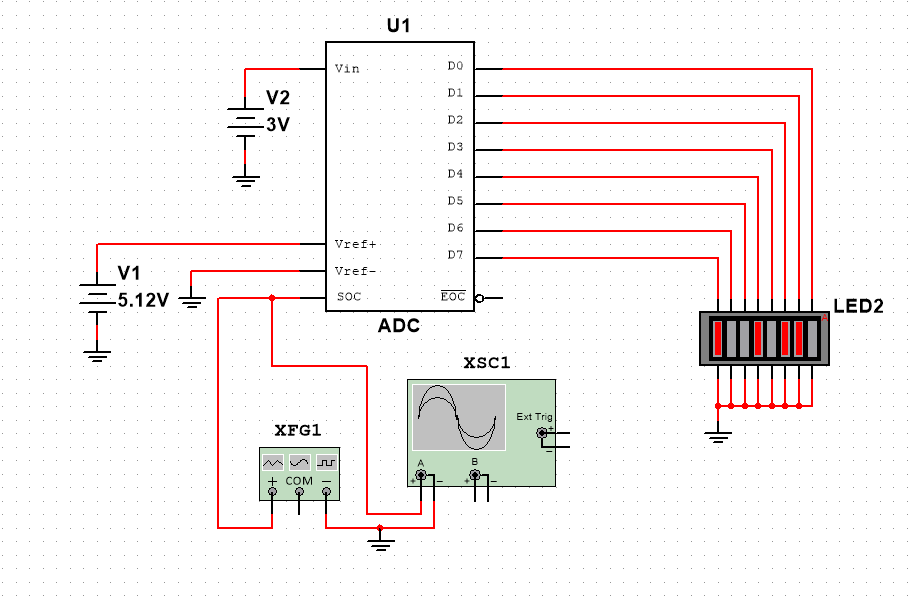
**Table 2. Components**

|  |  |  |
| --- | --- | --- |
| **Component Type** | **Quantity** | **Details** |
| IC | 1 | ADC0804 (8-bit µP Compatible Converter) |
| IC |  | LF398 Sample and Hold circuit |
| Capacitor |  | 100 pF |
| Capacitor |  | 150 pF |
| Capacitor |  | 10 µF (Tantalum) |
| Capacitor |  | 0.1 µF |
| Resistor |  | 1.3 kΩ |
| Resistor |  | 10 k ohm |
| LED display |  | 10-segment LED Bargraph (NSL5027 LEDs or equivalent) |

1. **INTRODUCTION**

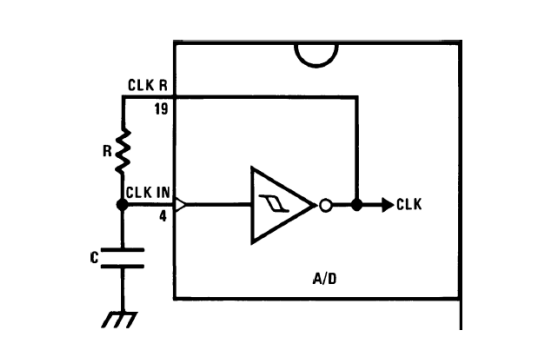
An analog to digital converter, also known as an ADC, does exactly how the name sounds. It takes an analog signal and converts it to digital for a microprocessor or another type of computer to use. This is done by performing holding and sampling and turning a sinusoidal wave (analog) into a piece wise function (digital). Sampling refers to when the IC takes a voltage reading at a certain point. Then, it will hold the reading there until there is enough of a drop or increase in voltage for it to sample again

1. **CIRCUIT DESCRIPTION**

Figure 1.

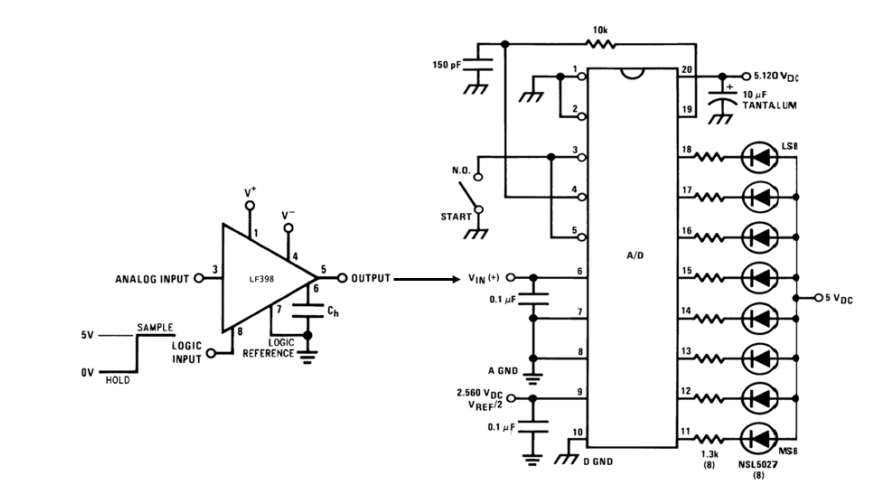
This figure shows the circuit configuration for the ADC tester with the LED bargraph display.

Figure 2.



Source: “Lab 2: Analog to Digital Converter”

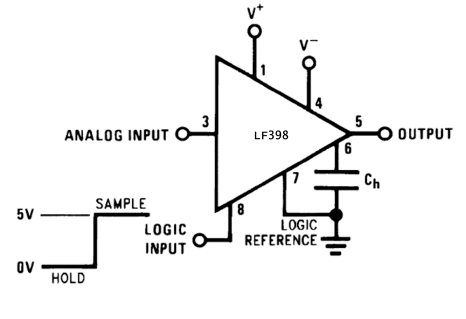
This figure shows the configuration of self-clock circuit of the ADC.

Figure 3.

Source: “Lab 2: Analog to Digital Converter”

This circuit schematic shows the configuration need for sampling an AC input signal with the ADC.

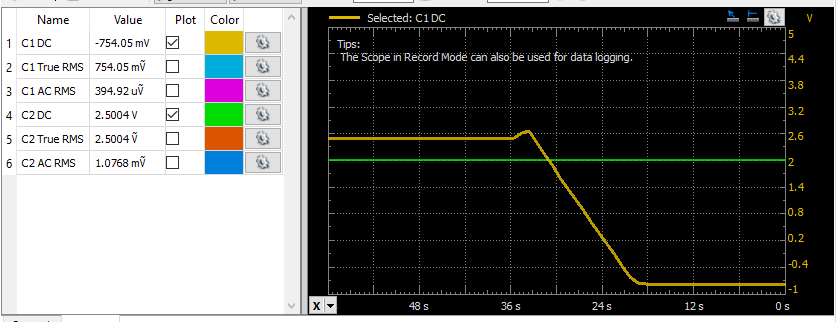
Figure 4.



Source: “Lab 2: Analog to Digital Converter”

This schematic shows the pinout of the LF398

Figure 5.

In the figure you can see the logger output decay of the hold/sample IC.

Graphical user interface

Description automatically generated Figure 6.

This figure shows the logger output with a slow sinewave input to the hold/sample IC.

1. **MEASUREMENTS**

Table 1. ADC output results

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Vin | Vin Measure | Bargraph output | | VMS Group | VLS Group | ADC Voltage Reading |
| 0 | -0.310 mV | 1111 | 1111 | 4.800 | 0.300 | 5.10 |
| 0.5 | 0.4930 V | 0110 | 0111 | 1.920 | 0.140 | 2.06 |
| 1.0 | 0.9920 V | 0011 | 0011 | 0.960 | 0.600 | 1.56 |
| 1.5 | 1.4930 V | 0100 | 1101 | 1.280 | 0.260 | 1.54 |
| 2.0 | 1.9930 V | 1001 | 1001 | 2.880 | 0.180 | 3.06 |
| 2.5 | 2.4993 V | 1111 | 1110 | 4.800 | 0.280 | 5.08 |
| 3.0 | 2.9939 V | 1010 | 0110 | 3.200 | 0.120 | 3.32 |
| 3.5 | 3.4940 V | 1101 | 0010 | 4.160 | 0.040 | 4.20 |
| 4.0 | 3.9940 V | 0100 | 1100 | 1.280 | 0.240 | 1.52 |
| 4.5 | 4.4940 V | 0001 | 1000 | 0.320 | 0.160 | 0.48 |
| 5.0 | 4.9950 V | 0000 | 0000 | 0 | 0 | 0 |

Listed in table 1 are my results from reading the bargraph of the ADC tester circuit (figure 1). As seen in the ADC voltage reading column, the results are inaccurate and nearly look to be inverted.

Table 2. Applying 2.5v to hold/sample chip pin #3

|  |  |  |
| --- | --- | --- |
| Pin#3 voltage | ADC bargraph Output | ADC output voltage |
| 0 | 01100110 | 2.8 + 0.18 = 2.89 V |
| 2.5 | 00011011 | 4.8 + 0.08 = 4.88 V |

Listed here are the differences of output on the bargraph display when a 2.5 V voltage is applied to the analog input of the LF398 hold/sample chip.

1. **DISCUSSION**

Looking at table 1, you will see something is off about the ADC voltage readings. These readings are a translation from the output of the bargraph. To perform this translation, one must invert the output before consulting the translation table to find the output. However, I had missed the step of taking the compliment of my outputs so, my conversions look to be in reverse for the 0.0 and 5.0 voltages specifically because they are each other’s compliment. I noticed this issue a few steps later and corrected myself from that point on, making note of it in my notebook.

In the next section of the laboratory experiment, section 8.1.7, we changed the clock value for the ADC by increasing the value of C in the RC circuit. R was 10K Ω and C was 150pF originally with a clock of frequency of 336.7KHz. Then, I changed it to 100pF giving me a new clock frequency of 450.3KHz, to which both frequencies fall in specification with the ADC clock frequency range on its datasheet.

The next part of this lab was to input an AC signal into the ADC. To do this a very slow input frequency of 0.5Hz, 1VP-P with an offset voltage of 0.5v (the positive offset is because the ADC cannot measure below 0v) was used. My observations of the bargraph output were that it changed rapidly, but not very quickly. I wrote in my notebook “It almost looks like it’s playing pong” and it went back and forth.

After that, the input frequency was increased to 1Hz, causing the bargraph to shift faster, making it difficult to read. The ADC will not be able to keep up after the input frequency reaches beyond its internal clock frequency for, the wave would shift too quickly, and the ADC would not be able to acquire an accurate measurement. The max clock frequency for this device is 1450KHz and the conversion time for the test circuit is between 103 and 114µs. I could not find the test circuit supply current, IS, on the datasheet.

Testing the ADC with a signal, the LF398 hold/sample circuit was built, and its output was connected to the input of the ADC. Here, we can look at the results from table 2, when a DC supply voltage of 2.5 volts was applied to pin 3 of the LF398.

Section 8.3.4 looks at pin 5 of the LF398 with an oscilloscope when sampling to see if it equals pin 3. When holding, pin 5 should be equal to pin 3. I was not seeing this equivalence at first, but after further investigation I found I had a grounding issue on the IC. I had the RC going to ground on their own instead of tying them together and then being grounded. After fixing this, I saw pin 5 match pin 3, and then once setting pin 8 to 0v, I saw a slow decay down. I was able to record this using the logger function on the analog discovery and it can be seen in figure 5. Adjusting the value of Ch would change the rate of decay (see figure 6).

For section 8.3.7, as noted during the question section of this report, I found it difficult to measure what the output voltage was and what the bargraph stated the output voltage was. The hold time was too short for me to gather all required data. However, the bargraph output declared the input to be 3.8v. In section 8.3.8, the output wave on the LF398 matched perfectly to the input wave during the sampling function of the chip.

1. **CONCLUSION**

In conclusion, ADCs and hold/sample ICs are very useful chips to have experience with for they have very real-world applications just as circuit board testers and more. During this lab, some of my measurements were off or did not look quite right. What I learned/relearned is that I need to take more time with reading through and fully understanding what do to before I go through and do it. For example, the results I find with the bargraph during the ADC tester look quite off and I made a note of it and moved on. However, later I came to find realize that the outputs of the ADC are “not-ed” meaning that they are the inverse. What this means is that I used the wrong values when performing my conversion on the table from the ADCs table sheet, but if I took some more time to absorb the procedure, this may have been avoided.

1. **QUESTIONS**

8.1.4 How accurate was your Analog to Digital conversion?

As previously stated in my discussion on the results in table 1, my conversions where not very accurate, but this was due to user error.

8.1.7 What is the frequency and is it withing the device specifications?

The frequency was 336.7KHz. This was withing device specs.

8.2.1 What does the LED bargraph display look like?

As previously noted, the LEDs changed very rapidly.

8.2.2 At what frequency will the A/D not be able to process the data?

After 1450KHz the A/D will not be able to process the data.

8.2.3.1 What is the conversion time with the test circuit clock frequency?

103 to 114µs

8.2.3.3 What is the max clock frequency that can be used?

1450KHz

8.2.5 What device would you add to the test circuit to make a better A/D converter?

I would add holding/sampling system, and buttons (which I did) to make it easier to reset/take samples between measurements.

8.3.4 How quickly does the output degrade? By changing the value Ch, does this change the timeframe that the value remains constant?

The stock time of decay is 18ms

8.3.7 Do these values match?

I was unable to get the voltage that the ADC would see because the hold time was not long enough to record the measurement.

8.3.8 Do these values match?

When sampling the wave, the output matches perfectly with the wave input.

1. **REFERENCES**
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3. Recitation Textbook
4. “Lab 2: Analog to Digital Converter.” *Lab2 Lab Procedure*, University of Massachusetts Lowell, 2021.